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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,496	06/30/2003	Jered Donald Aasheim	MS1-1466US	5314

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EXAMINER	
KIM, HAROLD J	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/610,496	AASHEIM ET AL.	
	Examiner	Art Unit	
	Harold Kim	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the filing of the Amendment on 9/28/2005. The arguments have been considered but they are not persuasive. Accordingly, this action is made **FINAL.**

2. Claims 1-34 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Cyran et al., US Pub. No.: US 2003/0191986 A1.

5. In re claim 1, Cyran et al. shows a processor-readable medium [fig 1C] comprising processor-executable instructions [figs 6 and 13] configured for:

identifying a plurality of respective states of applications [6008, fig 6; paragraph 0034, lines 5-10] having instructions executing on a processor [1500, fig 15; 1018, fig 1C], the respective states being identified over an interval of time [measure single range, fig 6];

receiving a plurality of instantaneous power consumption level indications over the interval of time [single range real-time, 6012, fig 6] from a power measurement circuit [6020, fig 6; 1022, fig 1C]; and

correlating ones of the instantaneous power consumption level indications with corresponding ones of the identified states of the applications [6020, fig 6; fig 13].

6. In re claim 2, Cyran et al. shows interrupting the processor [6002, fig 6];

sampling a program counter of the processor [1500, fig 15];

scanning a lookup table to find an address indicated by the program counter [6008, fig 6; 1500, fig 15], and

determining an instruction located at the address [1704, fig 17].

7. In re claim 3, Cyran et al. shows querying the power measurement circuit [6010, 6012, fig 6]; and

receiving digital power readings from the power measurement circuit based on the querying [6020, fig 6; fig 9; 1022 fig 1C; fig 13].

8. In re claim 4, Cyran et al. shows receiving digital power readings from the power measurement circuit at preset time intervals [1014, fig 1C].

9. In re claim 5, Cyran et al. shows the correlating comprises associating with an identified instruction, a measured amount of power consumed during execution of the identified instruction on the processor [fig 13].

10. In re claim 6, Cyran et al. shows the correlating comprises generating a power profile [fig 13] that includes a plurality of power consumption values [max power, avg power, fig 13] and a plurality of identified instructions [ReadNextData, ReadConstellation, fig 13], wherein each power consumption value is associated with an identified instruction in the power profile [fig 13].

11. In re claim 7, Cyran et al. shows a table [fig 13] having pairs of data, each pair of data comprising a power consumption value [Avg Power, fig 13] and an identified instruction [ReadNextData, fig 13]; and

a graph correlating power consumption values with identified instructions [fig 14].

12. In re claim 8, Cyran et al. shows power consumption values measured during execution of the instructions on the processor [target system processor, last 2 lines in Abstract].

13. In re claim 9, Cyran et al. shows a computer [1018].

14. In re claim 10, Cyran et al. shows a processor-readable medium [fig 1C] comprising processor-executable instructions [figs 6 and 13] configured for associating respective states of a software instruction [1500, fig 15; 1018, fig 1C; 6008, fig 6; paragraph 0034, lines 5-10] executed on a processor [CPU, fig 2] with corresponding indications of the amounts of power consumed instantaneously [real-time, 6012, fig 6] by executing the states of the software instruction [figs 13, 14].

15. In re claim 11, Cyran et al. shows generating a power profile [fig 13] that matches the respective states of the software instructions [6008, fig 6; paragraph 0034, lines 5-10] executing on an embedded device [1018, fig 1C] over an interval of time [fig 14; single range, 6012, fig 6] with corresponding instantaneous power consumption values [real-time, 6012, fig 6] measured during execution of the software instructions [last 2 lines of Abstract; fig 13] over the interval of time.

16. In re claim 12, Cyran et al. shows a processor-executable instructions [figs 6 and 13] configured for:

measuring over time a plurality of instantaneous power consumption levels [real-time, 6012, fig 6] associates with states of software instructions [6008, fig 6; paragraph 0034, lines 5-10] executing on a target computing device [6020, fig 6; 1022, fig 1C];

converting analog power measurements into digital power measurements [DSP in fig 1C]; and

transmitting the digital power measurements to a host computer [fig 1C].

17. In re claim 13, Cyran et al. shows processor-executable instructions configured for storing the digital power measurements in a memory after the converting [1022, fig 1C; fig 13].

18. In re claim 14, Cyran et al. shows receiving a request for the digital power measurements from the host computer [figs 1C, and 6]; and

transmitting the digital power measurements to the host computer based on the request [figs 1C and 6].

19. In re claim 15, Cyran et al. shows transmitting the digital power measurements to the host computer at preset time intervals [1014, fig 1C].

20. In re claim 16, Cyran et al. shows the target computing device is a computer [1018, fig 1C]

21. In re claim 17, Cyran et al. shows generating a power profile [fig 13] that associates, over an interval of time [single range, 6012, fig 6], respective states of software instructions with an amount of power instantaneously [real-time, 6012, fig 6] consumed during execution of the states of the software instructions [fig 13].

22. In re claim 18, Cyran et al. shows the execution of the software instruction is performed by a processor on a target computing device and the amount of power consumed is an amount of power consumed by the processor [fig 13; last 2 lines in Abstract].

23. In re claim 19, Cyran et al. shows identifying the software instruction executing on a processor [1500, fig 15; 1010, fig 1C];

receiving power consumption data from a power measurement circuit [6020, fig 6; 1022, fig 1C]; and

correlating the power consumption data with the identified software instruction [6020, fig 6; fig 13].

24. In re claim 20, Cyran et al. shows a computer comprising a power profiler [figs 1C, and 6] configured to identify state of software instructions executing on a processor [1500, fig 15; 1018, fig 1C], receive instantaneous [real-time, 6012, fig 6] power consumption data [6020, fig 6; 1022, fig 1C] corresponding to the states of the software instructions [6008, fig 6; paragraph 0034, lines 5-10], and correlate the instantaneous power consumption data with the states of the software instructions such that the states of the software instructions are associated with an instantaneous power consumption value indicating an amount of power consumed over time during the executing of the software instruction [6020, fig 6; fig 13].

25. In re claim 21, Cyran et al. shows a lookup table [6008, fig 6], the power profiler further configured to monitor a program counter on the processor [1500, fig 15] and to identify the software instructions through the lookup table based on the program counter

[1500, fig 15; 6008, fig 6].

26. In re claim 22, Cyran et al. shows a power profile [fig 13] having a plurality of power consumption values each paired with a

corresponding software instruction to indicate an amount of power consumed during execution of the corresponding software instruction [fig 13].

27. In re claim 23, Cyran et al. shows a computer [fig 1C] comprising a power profiler [fig 1C] configured to generate a power profile [fig 13] that correlates, over time [single range, 6012, fig 6], states of respective software instructions with instantaneous power consumption levels during execution of the software instructions.

28. In re claim 24, Cyran et al. shows a computer [fig 1C] comprising:

means for identifying states of applications having instructions executing on a processor [1500, fig 15; 1018, fig 1C; 6008, fig 6; paragraph 0034, lines 5-10]];

means for receiving instantaneous power consumption data [real-time, 6012, fig 6] from a power measurement circuit [6020, fig 6; 1022, fig 1C], and

means for generating a power profile that correlates the instantaneous power consumption data with the identified states of the instructions [6020, fig 6; fig 13, fig 14].

29. In re claim 25, Cyran et al. shows a computer [fig 1C] means for interrupting the processor [6002, fig 6];

means for sampling a program counter of the processor [1500, fig 15]; and

means for determining an instruction based on the program counter [1704, fig 17].

30. In re claim 26, Cyran et al. shows means for querying the power measurement circuit [6010, 6012, fig 6]; and

means for receiving digital power readings from the power measurement circuit based on the querying [6020, fig 6; fig 9; 1022, fig 1C; fig 13].

31. In re claim 27, Cyran et al. shows a power measurement circuit [fig 1C] comprising:

means for measuring instantaneous power consumption levels [real-time, 6012, fig 6] associated with states of software applications [6008, fig 6; paragraph 0034, lines 5-10] having instructions executing over time [single range, 6012, fig 6] on an embedded device [1022, fig 1C];

means for converting analog measurements of the instantaneous power consumption levels into digital representations [DSP, fig 1C], and

means for transmitting the digital representations to a host computer in response to a query from the host computer [fig 1C; 6020, fig 6].

32. In re claim 28, Cyran et al. shows means for storing the digital power measurements [fig 13].

33. In re claim 29, Cyran et al. shows a computer [fig 1C] comprising:

a processor [1018, fig 1C];

at least one application instruction stored in a memory and executable on the processor [1018, fig 1C; 6010, 6020, fig 6], and

a power measurement circuit [1022, fig 1C; 6020, fig 6] configured to measure,

over time [single range, 6012, fig 6], instantaneous power consumption levels [real-time, 6012, fig 6] associated with execution of at least one state of the application [6008, fig 6; paragraph 0034, lines 5-10].

34. In re claim 30, Cyran et al. shows an analog to digital converter integrated as part of the power measurement circuit [1022, fig 1C] and configured to convert analog power signals to digital power consumption data [DAP A/D, 1022, fig 1C].

35. In re claim 31, Cyran et al. shows a computer [1018, fig 1C].

36. In re claim 32, Cyran et al. show a system [fig 1C] comprising:

a power profiler [1002, fig 1C] configured to correlate, over time [single range, 6012, fig 6], at least one identified state of one of a plurality of software applications [6008, fig 6; paragraph 0034, lines 5-10] with an instantaneous power consumption level [real-time, 6012, fig 6] during execution of the identified state of the software application [6020, fig 6];

a lookup table having information for identifying the identified software application [6008, fig 6]; and

a power profile [fig 13] being generated by the power profiler and associating instantaneous power consumption values [real-time, 6012, fig 6] over time [single range, 6012, fig 6] with the identified states of the software applications [6010, fig 6], with the instantaneous power consumption value being paired with corresponding identified states of the software applications [6020, fig 6; fig 14].

37. In re claim 33, Cyran et al. shows a power measurement circuit [1022, fig 1C] configured to measure the amount of power consumed during execution of the identified

software instruction [6020, fig 6]; and

an analog to digital converter configured as part of the power measurement circuit to convert analog power consumption measurements into digital power consumption data [DSP (A/D), 1022, fig 1C; 6020, fig 6].

38. In re claim 34, Cyran et al. shows the power measurement circuit is a component [1010, fig 1C] of a target computing device [1018, fig 1C] on which the identified software instruction is executed.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive.

In the remarks, applicants argued in substance that Cyran does not show

identifying a plurality of respective states of applications having instructions executing on a processor, the respective states being identified over an interval of time;

receiving a plurality of instantaneous power consumption level indications over the interval of time from a power measurement circuit; and

correlating ones of the instantaneous power consumption level indications with corresponding ones of the identified states of the applications.

Examiner respectfully traverses applicants' remarks.

In the new ground of rejection as shown in above claim 1, Cyran shows identifying a plurality of respective states of applications [6008, fig 6; paragraph 0034,

lines 5-10] having instructions executing on a processor [1500, fig 15; 1018, fig 1C], the respective states being identified over an interval of time [measure single range, fig 6];

receiving a plurality of instantaneous power consumption level indications over the interval of time [single range real-time, 6012, fig 6] from a power measurement circuit [6020, fig 6; 1022, fig 1C]; and

correlating ones of the instantaneous power consumption level indications with corresponding ones of the identified states of the applications [6020, fig 6; fig 13].

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The centralized fax number is 571-273-8300.

The centralized hand carry paper drop off location is:

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401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application should be directed to the central telephone number (571) 272-2100.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harold Kim whose telephone number is 571-272-4148. The examiner can normally be reached on Monday-Thursday 6AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 571-272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HK

Harold J. Kim
Patent Examiner
December 12, 2005/HK

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